Claim(s)

What is claimed is:

1. An apparatus for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period T_P, the apparatus comprising:

first means for generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a first delay adjustable by first control data with a resolution of T_P/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one;

second means for generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M over a second range substantially wider than T_P/N, and

means for generating the first control data and the second control data in response to each pulse of the first pulse sequence.

2. The apparatus in accordance with claim 1 wherein M and N are relatively prime.

3. The apparatus in accordance with claim 1 wherein at least one of said first and second ranges is wider than T_P.

4. The apparatus in accordance with claim 1 wherein the first range is at least as wide as $(1 - 1/N)T_P$ and the second range is at least as wide as $(1 - 1/M)T_P$.

5. The apparatus in accordance with claim 4 wherein M and N are relatively prime.

6. The apparatus in accordance with claim 1 wherein the third pulse sequence is periodic.

7. The apparatus in accordance with claim 1 wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence, wherein each first gate has a switching delay of T_p/N.

8. The apparatus in accordance with claim 1 wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence, wherein each second gate has a switching delay of T_p/M.

9. The apparatus in accordance with claim 8 wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence,

wherein each second and third gate has a similar switching delay of T_p/M set by the magnitude of a second control signal applied to all of the second and third gates.

10. The apparatus in accordance with claim 9 wherein the second means further comprises means for monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the first control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

11. The apparatus in accordance with claim 1

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence,

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence,

wherein each first gate has a switching delay of T_p/N, and wherein each second gate has a switching delay of T_p/M.

12. The apparatus in accordance with claim 11 wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence, and

wherein each second and third gate has a similar switching delay of T_P/M set by the magnitude of a second control signal applied to all of the second and third gates.

13. The apparatus in accordance with claim 12 wherein the second means further comprises means for monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

14. The apparatus in accordance with claim 13

wherein said plurality of first gates includes N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence,

wherein the switching delay of each of said first gates is controlled by a magnitude of the first control signal supplied as input thereto, and

wherein the first means further comprises means for monitoring the first pulse sequence and the fifth pulse sequence and for adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

15. An apparatus for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than T_P, the apparatus comprising:

first means for generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a delay adjustable by first control data with a resolution of T_P/N,

second means for generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_p/M,

means for generating the first control data and the second control data in response to each pulse of the first pulse sequence, and

wherein M and N are relatively prime integers greater than one.

16. The apparatus in accordance with claim 15

wherein the first means comprises a plurality of first gates connected in series for generating pulses of the second pulse sequence in response to pulses of the first pulse sequence,

wherein the second means comprises a plurality of second gates connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence,

wherein each first gate has a switching delay of T_p/N, and wherein each second gate has a switching delay of T_p/M.

17. The apparatus in accordance with claim 16 wherein the second means further comprises M third gates connected in series for generating a fourth pulse sequence in delayed response to the first pulse sequence, and

wherein each second and third gate has a similar switching delay of T_p/M set by the magnitude of a second control signal applied to all of the second and third gates.

18. The apparatus in accordance with claim 17 wherein the second means further comprises means for monitoring the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

19. The apparatus in accordance with claim 18

wherein said plurality of first gates comprises N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence,

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto, and

wherein the first means further comprises means for monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence and for adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

20. A method for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than a period T_P, the method comprising the steps of:

a. generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a first delay adjustable by first control data with a resolution of T_P/N over a first range substantially wider than T_P/M, wherein M and N are differing integers greater than one;

b. generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M over a second range substantially wider than T_P/N, and

c. generating the first control data and the second control data in response to each pulse of the first pulse sequence.

21. The method in accordance with claim 20 wherein M and N are relatively prime.

22. The method in accordance with claim 20 wherein at least one of said first and second ranges is wider than T_p.

23. The method in accordance with claim 20 wherein the first and second ranges are each at least as wide as T_p.

24. The method in accordance with claim 23 wherein M and N are relatively prime.

25. The method in accordance with claim 20 wherein the third pulse sequence is periodic.

26. The method in accordance with claim 20 wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence, wherein each first gate has a switching delay of T_p/N.

27. The method in accordance with claim 20 wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence, wherein each second gate has a switching delay of T_p/M.

28. The method in accordance with claim 27 wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence, wherein each second and third gate has a similar switching delay of T_p/M set by a magnitude of a control signal applied to all of the second and third gates.

29. The method in accordance with claim 28 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence, and

b2. adjusting the magnitude of the control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

30. The method in accordance with claim 20

wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence,

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence,

wherein each first gate has a switching delay of T_p/N, and wherein each second gate has a switching delay of T_p/M.

31. The method in accordance with claim 30 wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence, wherein each second and third gate has a similar switching delay of T_p/M set by the magnitude of a second control signal applied to all of the second and third gates.

32. The method in accordance with claim 31 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence, and

b2. adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

33. The method in accordance with claim 32

wherein said plurality of first gates comprises N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence,

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto,

wherein step a comprises the substeps of:

a1. monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence, and

a2. adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.

34. A method for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_P, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than T_P, the method comprising the steps of:

a. generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a delay adjustable by a first control data with a resolution of T_P/N,

b. generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_P/M,

c. generating the first control data and the second control data in response to each pulse of the first pulse sequence, and

wherein M and N are relatively prime integers greater than one.

35. The method in accordance with claim 34

wherein step a comprises applying the first pulse sequence as input to a plurality of first gates connected in series so that the first gates generate pulses of the second pulse sequence,

wherein step b comprises applying the second pulse sequence as input to a plurality of second gates connected in series so that the second gates generate pulses of the third pulse sequence,

wherein each first gate has a switching delay of T_p/N, and wherein each second gate has a switching delay of T_p/M.

36. The method in accordance with claim 35 wherein step b comprises applying the first pulse sequence as input to M third gates connected in series so that the third gates generate pulses of a fourth pulse sequence in delayed response to the first pulse sequence, wherein each second and third gate has a similar switching delay of T_p/M set by the magnitude of a second control signal applied to all of the second and third gates.

37. The method in accordance with claim 36 wherein step b comprises the substeps of:

b1. monitoring a phase relationship between the first pulse sequence and the fourth pulse sequence, and

b2. adjusting the magnitude of the second control signal so that the fourth pulse sequence is phase-locked to the first pulse sequence.

38. The method in accordance with claim 37

wherein said plurality of first gates comprises N first gates connected in series and delaying the first pulse sequence to produce a fifth pulse sequence,

wherein the switching delay of each of said first gates is controlled by a magnitude of a first control signal supplied as input thereto,

wherein step a comprises the substeps of:

a1. monitoring a phase relationship between the first pulse sequence and the fifth pulse sequence, and

a2. adjusting the magnitude of the first control signal so that the fifth pulse sequence is phase-locked to the first pulse sequence.